台揚科技股份有限公司
MICROELECTRONICS TECHNOLOGY INC.

ISO 9001 Certified

MTI MSx10 RFID Reader SiP Datasheet

Version 1.2a

IMPINJ CONNECTED

Contents

OVERVIEW

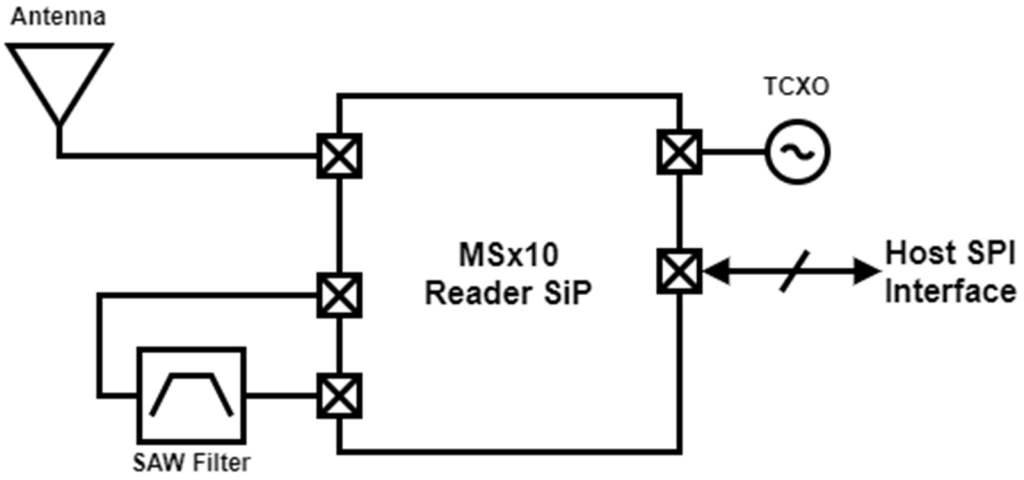
This document constitutes the preliminary and confidential electrical, mechanical, and thermal specifications for MTI MSx10 SiP. It contains a functional overview, mechanical characteristics, package signal locations, and targeted electrical specifications.

Overviews of the capabilities of the MSx10 SiP are shown in Table 1, and a reader system block diagram is shown in Figure 1.

Table 1: MSx10 Reader SiP Overview

Parameter	Description
Air Interface Protocol	EPCglobal UHF Class1 Gen 2 / ISO 18000-63
Transmit Output Power	Configurable up to +11ddBm at YK_TO pin, internal PA output power up to +27 dBm at PA_TO pin (External power amplifier supported for high performance applications, up to 33 dBm total Tx Power)
Receive Sensitivity	● MS710: -88dBm ● MS510: -82dBm ● MS310: -75dBm Note: all values with +10 dBm self-jammer, in FCC DRM RF Mode (20 µs TARI, 250 kHz BLF, Miller-4) at RX pin
Opearating Frequencies	860~930MHz
Supported Regions	All worldwide regions supported, including: ● US, Canada, and other regions following US FCC 47 CFR Ch. 1 Part 15 ● Europe and other regions following ETSI EN 302 208-1 (V 2.1.1) ● China, Japan, and other worldwide regions
Integration	● Embedded Impinj Ex10 contained RAIN Radio, Modem, MAC, RF Baluns, and Power Detectors ● Integrated RF front end contained high power ampilfier, directional coupler ● Integrated decoupling capacitors ● Integrated PLL loop filter
Power	Power consumption with internal PA at +25dBm ● Active at 3.3V : -VDD (VDD_ANA/DIG/SUP/IO_FLASH) :1000 mW -VCC_PA, 1700mW
Package Type	68 pin 11mm*11mm LGA, 1.4 mm thickness

Figure 1 – MSx10 SiP-based Circuita Block Diagram



1 INTRODUCTION

The MTI MSx10 is Impinj Ex10 based RFID reader SiPs, it is a highly integrated, high-performance for EPC Gen2 / ISO18000-63 UHF RFID applications. The reader SiP is implements direct conversion receiver architecture, and operates in the worldwide UHF industrial, science, and medical (ISM) band. The highly integrated reader SiP contains most of the necessary components into a tiny package, including all the RF and baseband blocks to interrogate and receive data from compatible RAIN tags, and an integrated microcontroller with embedded RAIN firmware providing the GS1 UHF Gen2 RAIN protocol as a pre-integrated feature.

1.1 Features

- Impinj Ex10 reader die
  - Modem architecture uses modern digital signal processing
  - Self-Jammer Cancellation Technology
  - Fully integrated voltage-controlled oscillator (VCO) with worldwide RFID coverage
  - Integrated Power Amplifier (PA) and baluns
  - High compression point quadrature downconverting mixer
  - Integrated RF envelope detectors for forward- and reverse- power sensing
  - Integrated Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs)
  - Configurable digital baseband
  - Integrated ARM Cortex-M0+ microcontroller core with embedded firmware
  - SPI host interface up to 4 MHz
- RF front end
  - High Isolation directional coupler
  - Integrated High Power Amplifier (PA) up to 27dBm (Conditional Bias)

- Support both Bi-static and Mono-static
- LO Attenuator

- Integrated PLL loop filter
- Capacitors for blocking, decoupling, and bypass for Impinj Ex10

1.2 Reference Documents

The conventions used in the UHF Gen2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this MSx10 Reader SiP Datasheet. Users of this datasheet should familiarize themselves with the UHF Gen2 Specification.

The MSx10 is fully compliant with the protocol specifications and local regulation documents in Table 2:

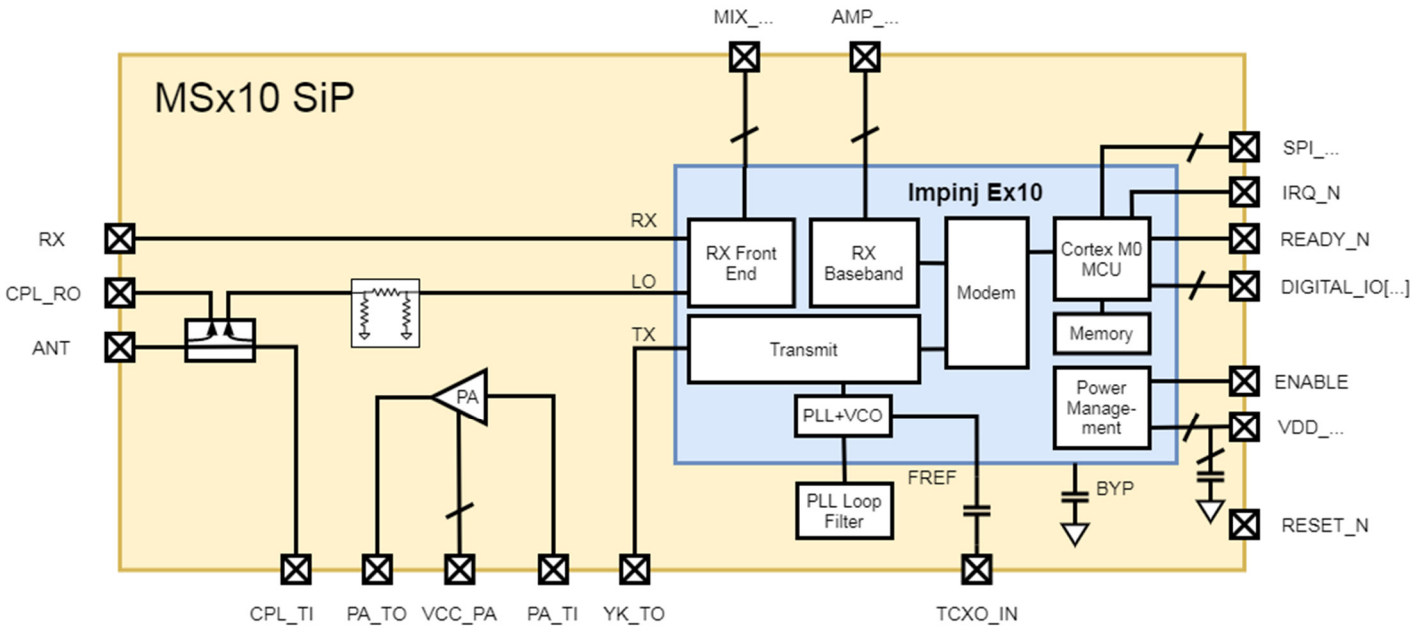
Table 2: Specification Documents

Protocol Specification Documents	• GS1 EPCGlobal Interoperability Test System for EPC compliant Class-1 Gen-2 UHF RFID
Local Regulation Documents	• FCC 47 CFR Ch. 1, part 15 • ETSI EN 302 208-1 V 2.1.1

1.3 Block Diagram

Figure 2 contains a detailed internal block diagram of the MSx10. The core of MSx10 SiP is built in Impinj Ex10 with periphael RF front end and power circuits to minize the design effort to develop the Rain RFID reader. MSx10 is fully compliant with the protocol specifications and local regulation documents in Table 2:

Figure 2 – MTI MSx10 Detailed Internal Block Diagram



2 SPECIFICATIONS

2.1 Pin Listing and Signal Definitions

The MSx10 is offered in a 68-pin 11*11 mm LGA package. The pinout for the 11x11 mm LGA is shown graphically in Figure 3 and in a list in Table 3. For package dimensions, see section 4.1 - Package Dimensions.

Figure 3 – MTI MSx10 Pinout

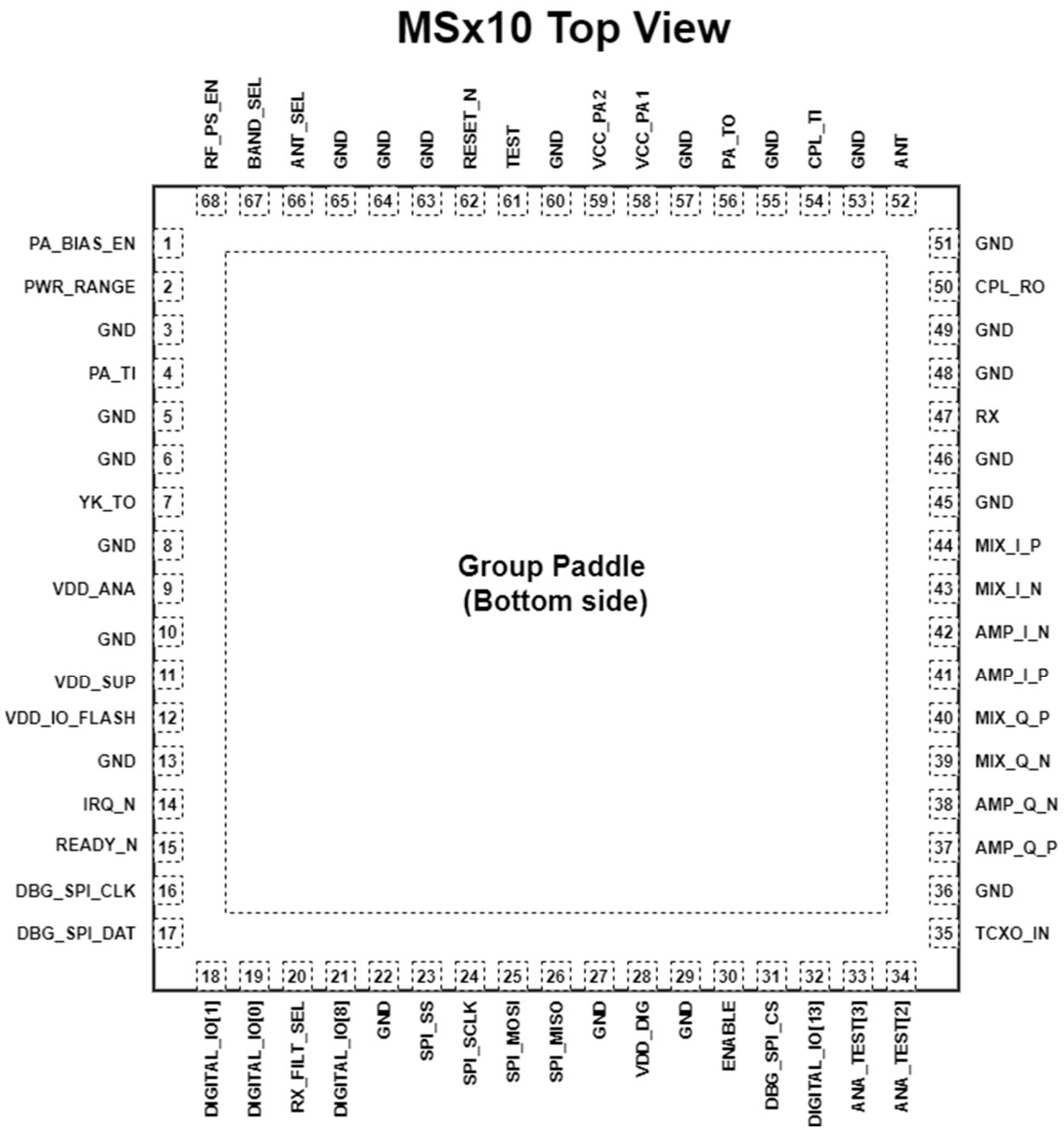


Table 3: MTI MSx10 Signal Listing

Pin #	Pin number	Signal Type	Description
1	PA_BIAS_EN	Digital Output	INT/EXT PA Selection 1.For internal or external PA selection as output indicator and it's associated to PA bias enable (reference design) 2. Configurable Digital_IO[16]
2	PWR_RANGE	Digital IO	1. For external PA BIAS range (reference design) 2. Configurable Digital_IO[15]
3	GND	GND	Ground
4	PA_TI	RF IN	Internal PA RF transmit signal input
5	GND	GND	Ground
6	GND	GND	Ground
7	YK_TO	RF OUT	Impinj Ex10 RF transmit signal output
8	GND	GND	Ground
9	VDD_ANA	Power Supply	Analog power supply
10	GND	GND	Ground
11	VDD_SUP	Power Supply	Supervisory power supply
12	VDD_IO_FLASH	Power Supply	Digital IO and Flash memory power supply
13	GND	GND	Ground
14	IRQ_N	Digital Output	Interrupt signal output (active low)
15	READY_N	Digital IO	SPI slave ready signal output (active low), boot to application/bootloader pin
16	DBG_SPI_CLK	Digital Output	Debug SPI Master Clock
17	DBG_SPI_DAT	Digital Output	Debug SPI Master MOSI (data out)
18	DIGITAL_IO[1]	Digital IO	Digital input/output (Debug SWDIO functionality for Impinj usage only)
19	DIGITAL_IO[0]	Digital IO	Digital input/output (Debug SWCLK functionality for Impinj usage only)
20	RX_FILT_SEL	Digital IO	1. For exteranl RX DRM filter selection (reference design) 2. Configurable Digital_IO[7]
21	DIGITAL_IO[8]	Digital IO	Digital input/output
22	GND	GND	Ground
23	SPI_SS	Digital Input	SPI slave select (active low)
24	SPI_SCLK	Digital Input	SPI clock
25	SPI_MOSI	Digital Input	SPI master output slave input
26	SPI_MISO	Digital Output	SPI master input slave output
27	GND	GND	Ground
28	VDD_DIG	Power Supply	Digital Power supply
29	GND	GND	Ground
30	ENABLE	Digital Input	SiP enable input
31	DBG_SPI_CS	Digital Output	Debug SPI Master Chip Select
32	DIGITAL_IO[13]	Digital IO	Digital input/output
33	ANA_TEST[3]	ANALOG IO	Analog test signal
34	ANA_TEST[2]	ANALOG IO	Analog test signal

Pin #	Pin number	Signal Type	Description
35	TCXO_IN	Clock Input	24 MHz PLL reference clock signal
36	GND	GND	Ground
37	AMP_Q_P	Analog Input	Q post-mixer amplifier quadrature differential input (positive)
38	AMP_Q_N	Analog Input	Q post-mixer amplifier quadrature differential input (negative)
39	MIX_Q_N	Analog output	Q mixer quadrature differential output (negative)
40	MIX_Q_P	Analog output	Q mixer quadrature differential output (positive)
41	AMP_I_P	Analog Input	I post-mixer amplifier quadrature differential input (positive)
42	AMP_I_N	Analog Input	I post-mixer amplifier quadrature differential input (negative)
43	MIX_I_N	Analog output	I mixer quadrature differential output (negative)
44	MIX_I_P	Analog output	I mixer quadrature differential output (positive)
45	GND	GND	Ground
46	GND	GND	Ground
47	RX	RF	RFID receive signal
48	GND	GND	Ground
49	GND	GND	Ground
50	CPL_RO	RF OUT	Coupler RF RX output , optional for Bi-static if connected to 50 ohm terminal
51	GND	GND	Ground
52	ANT	RF OUT	Ant Port
53	GND	GND	Ground
54	CPL_TI	RF IN	Coupler RF TX input
55	GND	GND	Ground
56	PA_TO	RF OUT	Internal PA RF transmit signal output
57	GND	GND	Ground
58	VCC_PA	Power Supply	PA power supply
59	VCC_PA	Power Supply	PA power supply
60	GND	GND	Ground
61	TEST	DNU	Reserved for Impinj usage only. Should be tied to ground.
62	RESET_N	Digital IO	SiP reset signal (active low)
63	GND	GND	Ground
64	GND	GND	Ground
65	GND	GND	Ground
66	ANT_SEL	Digital IO	1. For exteranl antenna selection(reference design) 2. Configurable Digital_IO[19]
67	BAND_SEL	Digital IO	1. For exteranl sawifilter selection(reference design) 2. Configurable Digital_IO[18]
68	RF_PS_EN	Digital IO	1. For exteranl Power enable(reference design) 2. Configurable Digital_IO[17]
Paddle	GND	GND	SiP GND

2.2 IO Connections and Configurations

The MSx10 has a number of input and output pins that are used to configure the device. A host device such as an MCU or an embedded computer can control and monitor these pins. This section enumerates the required, recommended, and optional connections, and gives notes on their states.

MSx10 (Impinj Ex10 based) SiP firmware currently doesn't support using the DIGITAL_IO pins as inputs. This feature may be added in a future firmware release.

2.2.1 Digital IO Default Drive Modes

The MSx10 SiP digital IOs start up in either a pull-up or pull-down drive mode. The DIGITAL_IOs can be reconfigured using the reader chip firmware operations, but at startup, their drive modes will be as shown in Table 4. The IO pull-up and pull-down resistance is specified in Table 17.

Table 4: MTI MSx10 Digital IO Default Drive Modes

Pin #	Pin Name	Type	Default Drive Mode	Impinj Ex10's GPIO
1	PA_BIAS_EN	Digital IO	Pull-up	DIGITAL_IO[16]
2	PWR_RANGE	Digital IO	Pull-up	DIGITAL_IO[15]
18	DIGITAL_IO[1]	Digital IO	Pull-up	DIGITAL_IO[1]
19	DIGITAL_IO[0]	Digital IO	Pull-up	DIGITAL_IO[0]
20	RX_FILT_SEL	Digital IO	Pull-up	DIGITAL_IO[7]
21	DIGITAL_IO[8]	Digital IO	Pull-up	DIGITAL_IO[8]
32	DIGITAL_IO[13]	Digital IO	Pull-up	DIGITAL_IO[13]
61	Test	DNU	Pull-down	Test
62	RESET_N	Digital Input	Pull-up	RESET_N
66	ANT_SEL	Digital IO	Pull-up	DIGITAL_IO[19]
67	BAND_SEL	Digital IO	Pull-up	DIGITAL_IO[18]
68	RF_PS_EN	Digital IO	Pull-up	DIGITAL_IO[17]

2.2.2 Host IO Connections

Table 5: MTI MSx10 Host Device Connections

Category	Pin Name	Type	Connection	Notes
SPI (Serial Peripheral Interface)	SPI_SS	Digital Input	Required	SPI slave select (active low) Required for SPI communication with the host.
	SPI_SCLK	Digital Input	Required	SPI clock Required for SPI communication with the host.
	SPI_MOSI	Digital Input	Required	SPI master output slave input Required for SPI communication with the host.
	SPI_MISO	Digital Output	Required	SPI master input slave output Required for SPI communication with the host.
	READY_N	Digital IO	Required	SPI slave ready signal output (active low), startup boot to application/bootloader pin Required for SPI communication with the host.
Firmware State	IRQ_N	Digital Output	Recommended	Interrupt signal output (active low) Indicates to the host when data is ready on the Mx10 SiP. Can be left unconnected if host queries the Mx10 SiP regularly.
SiP Control	ENABLE	Digital Input	Required	SiP enable input Allows host to control startup and put chip in a low power mode. Details on control below.
	RESET_N	Digital Input	Required	SiP reset signal (active low) Allows host to reset the Mx10 SiP without cycling the power. Must be sequenced as described in the next section. The Mx10 SiP drives this signal strong low during startup, so it must not be driven strong high externally.

2.2.3 IO Conditions

Certain MSx10 SiP IOs must be in a certain electrical state for specific optional or mandatory operational states. They are listed below. These are in addition to the power supply pins, RF and baseband interface pins, etc. More details on startup sequence timing are shown in section 2.3.1 - Startup Conditions.

ENABLE must be driven high to enable the MSx10 SiP. It should only be driven high after a stable 24 MHz clock signal is present at the TCXO_IN pin. ENABLE may be driven low to put the part into “Shutdown” mode.

RESET_N must be driven strong low at the start of MSx10 startup. It should be released 500 µs after the ENABLE pin is driven high. An internal pull-up resistor will pull the pin high. RESET_N may be used to reset the MSx10 SiP during operation.

READY_N must be driven strong low for 8706 FREF clock cycles (~362.75 µs) at startup (after the ENABLE pin goes high) to force the MSx10 into bootloader mode. During a normal startup to application (not to bootloader) the READY_N pin will be driven low by MSx10 to indicate that startup has completed, and the MSx10 is ready to communicate with the host via the SPI. Interface. The READY_N pin is also part of the SPI signaling wireline.

2.3 Power Supply

The MSx10 has multiple power supply pins, and to achieve maximum performance, they must be properly configured. A block diagram of the reader SiP power supplies is shown in Figure 4.

VDD_ANA, VDD_DIG, VDD_SUP, and VDD_IO_FLASH supply internal Impinj Ex10 . VCC_PA supplies internal high power amplifier.

Figure 4 – MTI MSx10 Power Supply Block Diagram

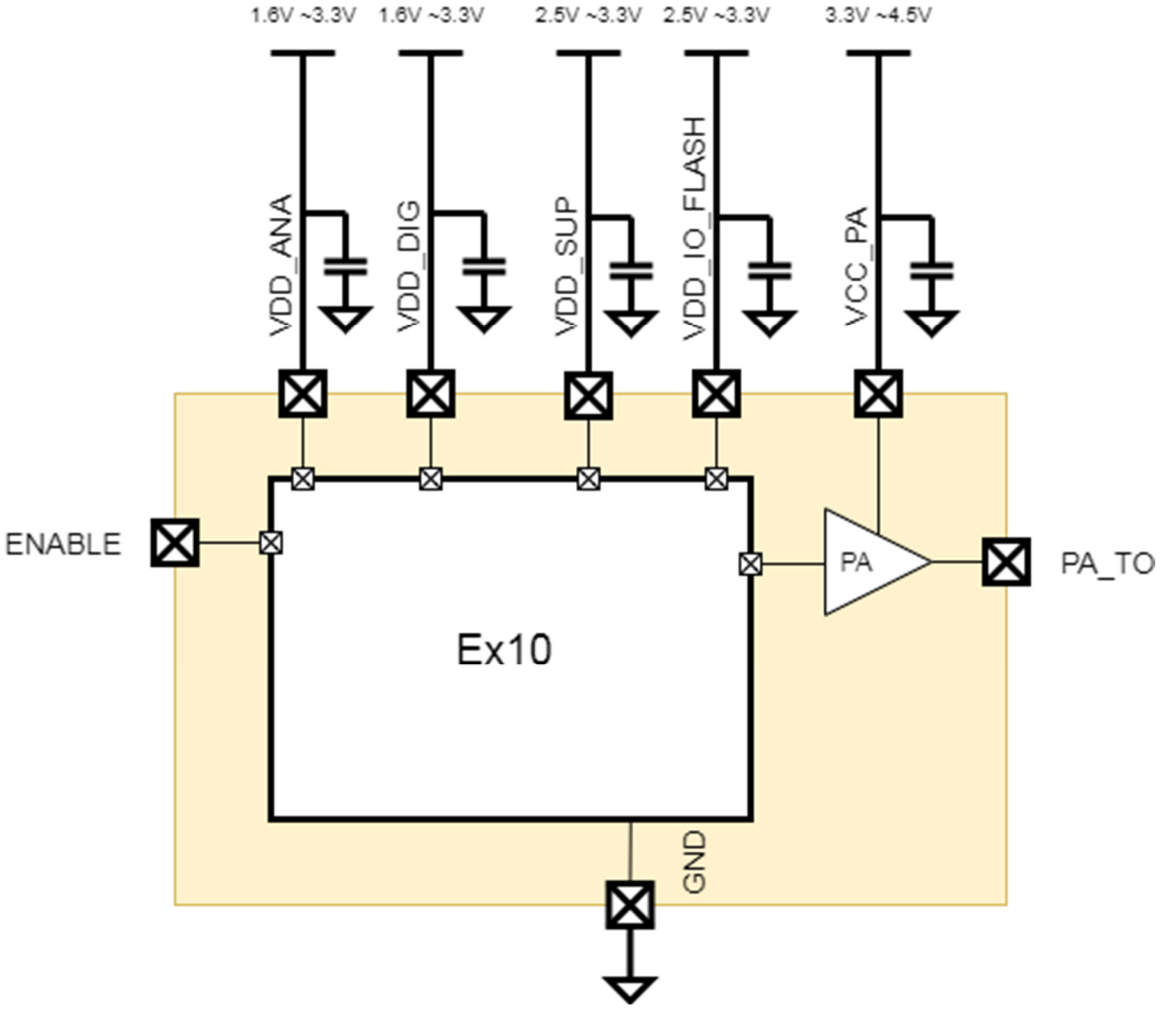
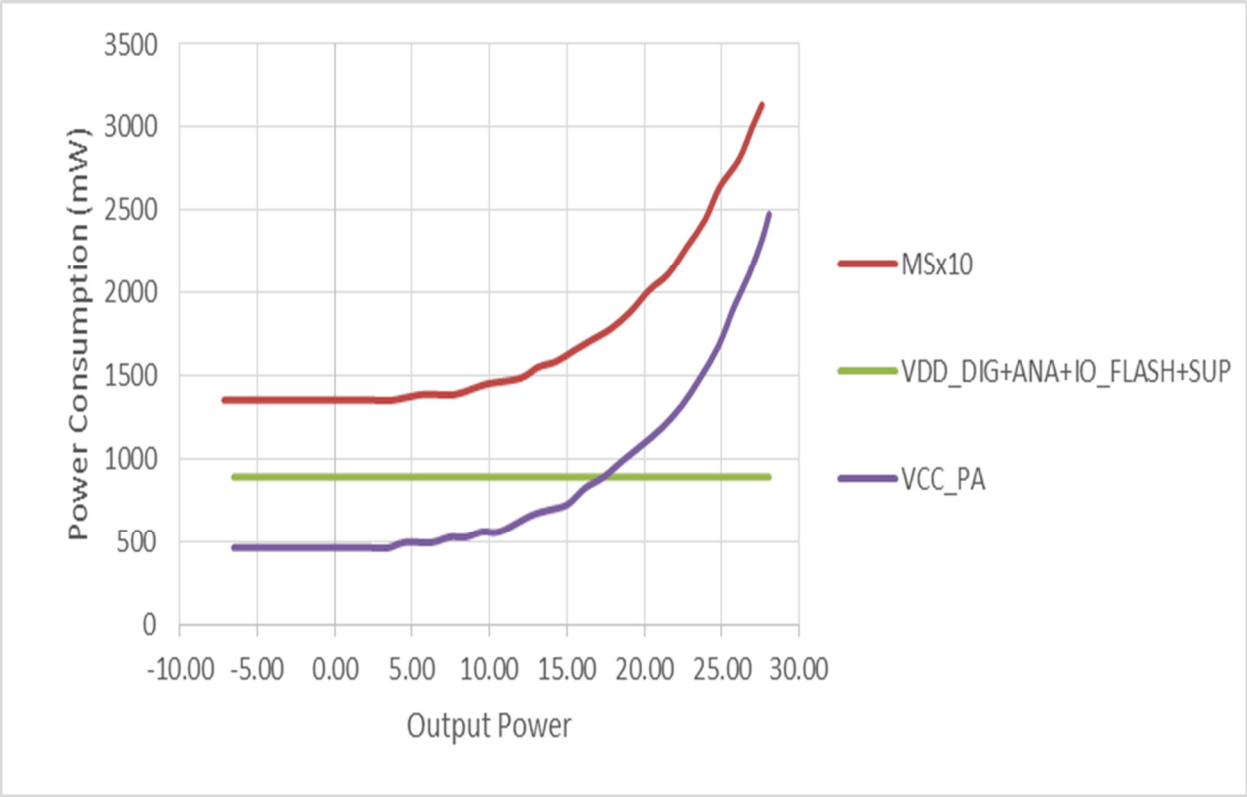


Figure 5 – MTI MSx10 Power Consumption



Note: Test with 3.3V single bias at CW mode

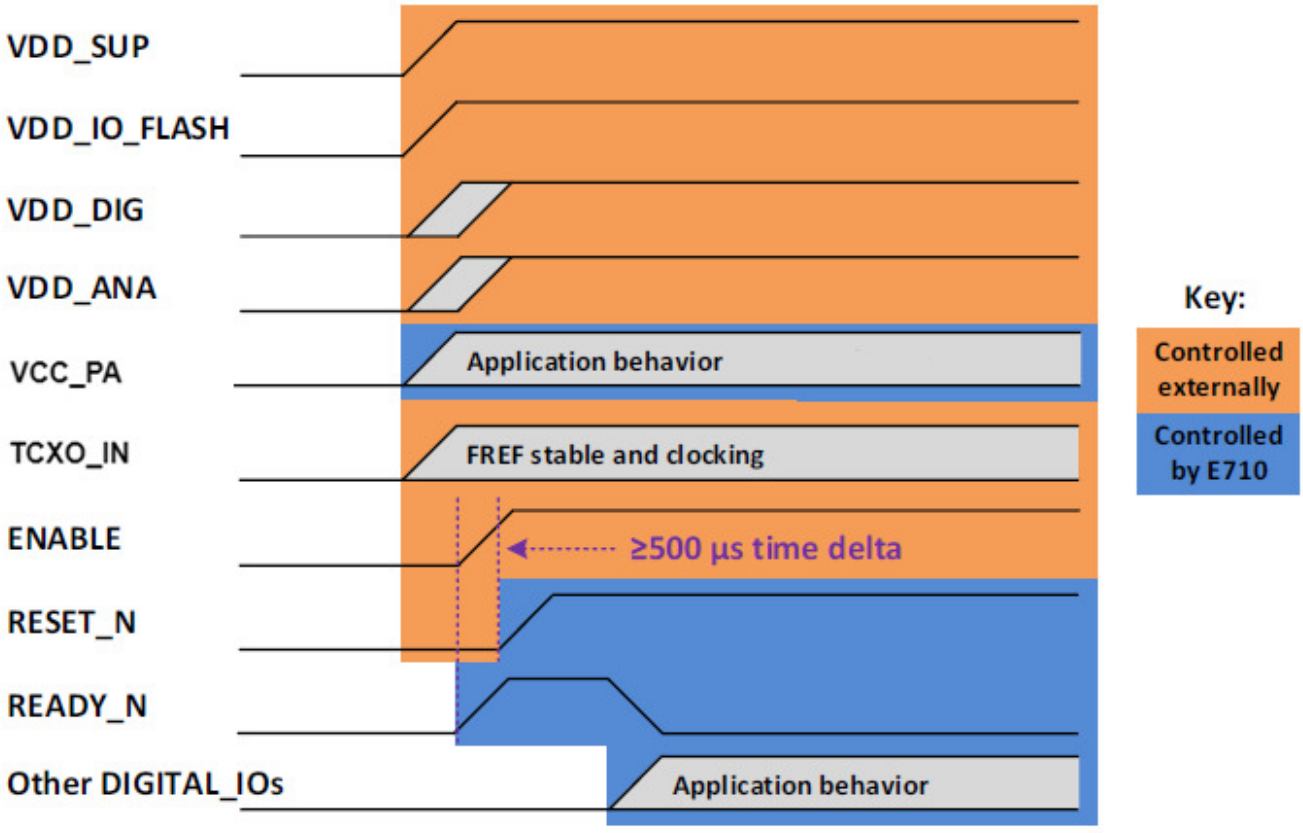
2.3.1 Startup Conditions

The power-on sequence must power the VDD_DIG and VDD_ANA supplies either simultaneously with, or after the VDD_SUP, VDD_IO_FLASH power supplies. The VDD_DIG and VDD_ANA supplies must not be powered up before the other power supplies on the device. A 24 MHz clock must be present at TCXO_IN for the part to start up successfully. The part will not startup if the ENABLE pin is not high, or if the RESET_N pin is not allowed to be driven low by the MSx10. Approximately 500 µs after the enable pin goes high, the part will release the RESET_N pin, and firmware startup will begin. The READY_N pin will be driven low by the MSx10 SiP when firmware startup has completed, and the part is ready to communicate via SPI with the host device. The READY_N pin may also be driven high at startup to force the part into the bootloader mode. For more details on this, see section 2.2.2 - IO conditions.

For more detail on startup, including detail on how to boot to the bootloader, see the firmware HTML documentation.

1. Power the reader chip
    a. VDD_SUP, and VDD_IO_FLASH should be powered up before or simultaneously with VDD_DIG and VDD_ANA
    b. A 24 MHz clock signal should be applied to TCXO_IN simultaneously or after power is applied
2. Apply IO conditions to startup the chip
    a. RESET_N must be left floating by the host
    b. ENABLE should be driven high by the host
    c. All other IOs should be left floating
    d. After approximately 500 µs, the RESET_N pin will be driven high by the reader chip, and firmware startup will begin
3. Observe the conclusion of startup
    a. When the READY_N pin is driven low by the chip, firmware startup has completed
    b. At this point, the chip firmware will respond to SPI commands, and all the DIGITAL_IOs can be used for other purposes
    c. The ENABLE pin should still be driven high, and RESET_N should be left floating during operation

Figure 6 – MTI MSx10 Power Supply and IO Sequencing

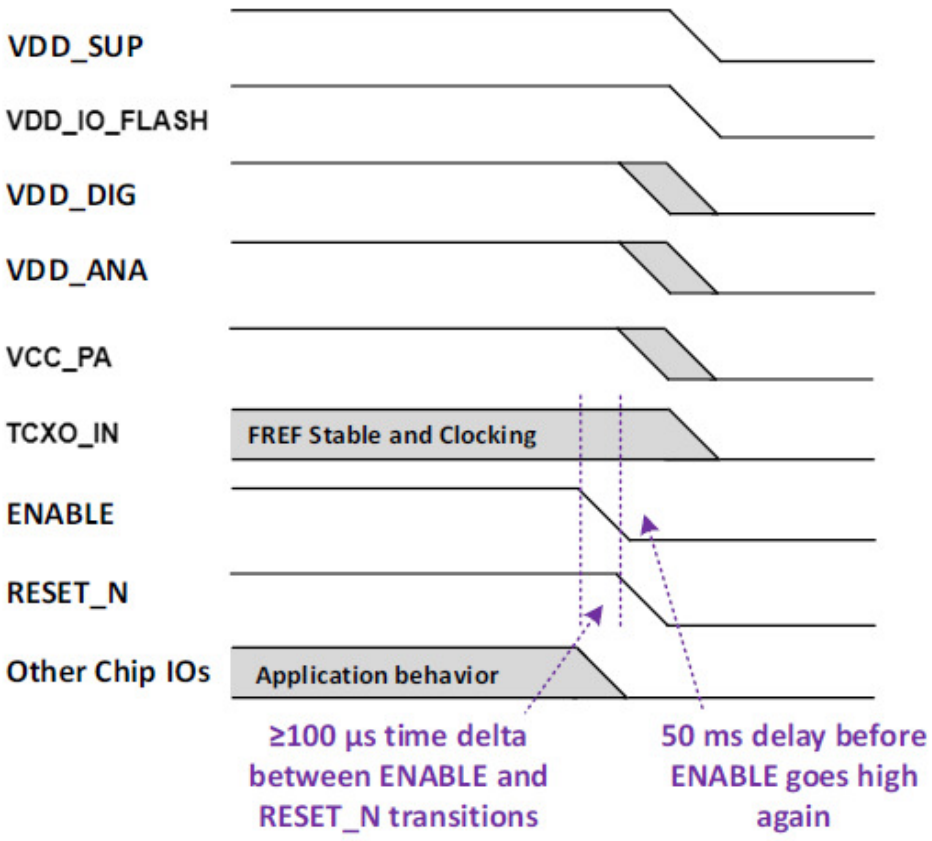


2.3.2 Power Down Sequence

The MTI MS710, E510, and E310 reader SiPs must be powered down in a specific sequence. That sequence is described in detail below and shown in Figure 7.
Note: It is critical that the ENABLE pin goes low 100 µs before RESET_N transitions low or power is removed from the SiP. If this condition is not met, the chip could enter a state that is only recoverable through a chip power cycle.

1. Disable the chip
    a. The chip can be disabled by driving the ENABLE pin low
        i. At this point, the chip will stop responding to SPI communication, and application driven IO behaviors will cease
    b. The ENABLE pin must be driven low for 100 µs before the chip is reset or powered down
        i. The 24MHz reference frequency (TCXO_IN) input must continue clocking until this 100 µs delay has completed
2. Reset and power down the chip
    a. All chip IOs should either be left floating(high impedance) or driven to ground
    b. FREF may stop clocking
    c. The RESET_N pin may be driven low
    d. The VDD pins may be driven low, which will also drive RESET_N low if it is floating
        i. VDD_DIG and VDD_ANA should be driven low either before or simultaneously with VDD_SUP and VDD_IO_FLASH
3. The chip should be left powered down for at least 50 ms before it is powered up again

Figure 7 – MTI MSx10 Power Down Sequence

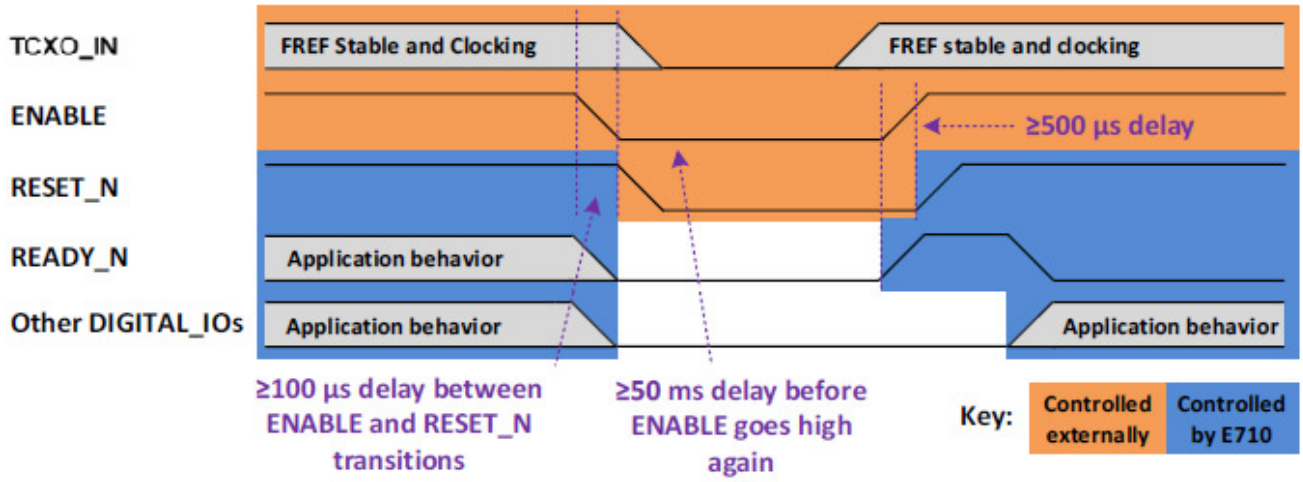


2.3.3 Disable-Enable Sequence

The MTI MS710, MS510, and MS310 reader chips must be disabled and re-enabled in a specific sequence. That sequence is described in detail below and shown in Figure 8.
The Disable functionality allows reduced power consumption without removing power from the reader chip. Reader designs should still maintain the ability to power down the chip to resolve unrecoverable states.
Note: It is critical that the ENABLE pin goes low 100 µs before RESET_N transitions low. If this condition is not met, the chip could enter a state that is only recoverable through a chip power cycle.

1. Disable the chip
    a. The chip should be disabled by driving the ENABLE pin low
        i. At this point, the chip will stop responding to SPI communication, and application driven IO behaviors will cease
    b. The ENABLE pin must be driven low for 100 µs before the RESET_N pin is driven low
        i. The 24MHz reference frequency (TCXO_IN) input must continue clocking until this 100 µs delay has completed
2. Reset the chip
    a. All chip IOs should either be left floating (high impedance) or driven to ground
    b. FREF may stop clocking
    c. The RESET_N pin should be driven low
3. Chip disabled
    a. At this point, the chip is disabled, and will consume reduced current
    b. The chip must be left disabled for at least 50 ms before it is enabled again
4. Apply IO conditions to re-enable the chip
    a. FREF must be stable and clocking before any other IO conditions are changed
    b. RESET_N must be left floating by the host
    c. ENABLE should be driven high by the host
    d. All other IOs should be left floating
    e. After approximately 500 µs, the RESET_N pin will be driven high by the reader chip, and firmware startup will begin
5. Observe the conclusion of startup
    a. When the READY_N pin is driven low by the chip, firmware startup has completed
    b. At this point, the chip firmware will respond to SPI commands, and all of the DIGITAL_IOs can be used for other purposes
    c. The ENABLE pin should still be driven high, and RESET_N should be left floating during operation

Figure 8 – MTI MSx10 Disable_Enable Sequence



2.4 Electrical Specifications

Note: Blank cells in the Minimum, Typical, or Maximum columns indicate specs are to be determined (TBD).

The MTI MSx10 is an Impinj Ex10 based RFID reader SiP. The most of electrical specifications are accosiated with Impinj Ex10 specifications. If the specifications are not described in below, please see the detail in Impinj Ex10 datasheet.

2.4.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 5 define limitations for electrical and thermal stresses. These limits prevent permanent damage to the MTI MSx10 reader SiP. If the SiP is exposed to conditions outside of these ranges, it is no longer guaranteed to operate properly or meet the performance specifications listed in this document.

Table 6: Absolute Maximum Ratings

Parameter	Min	Max	Unit	Conditions
VDD_SUP/IO_FLASH voltage	-0.3	3.6	volts DC	
VDD_DIG/_ANA voltage	-0.3	3.6	volts DC	
VCC_PA	-0.3	5.25	volts DC	
Chip IO applied voltage	-0.3	3.6	volts DC	
ESD, Power supply and IO pins	N/A	N/A	volts peak	Electro-static Discharge, HBM Class 3A
	N/A	N/A	volts peak	Electro-static Discharge, CDM Class C2
ESD, RF pins	N/A	N/A	volts peak	Electro-static Discharge, HBM Class 3A
	N/A	N/A	volts peak	Electro-static Discharge, CDM Class C2
PA_TI port RF input power	N/A	10	dBm	
CPL_TI port RF input power	N/A	33	dBm	
RX port RF input power	N/A	20	dBm	
Storage Temperature	-55	125	°C	
Case Temperature	N/A	260	°C	For reflow purposes

2.4.2 Operating Conditions

The operating conditions listed in this section describe the conditions under which the MSx10 will operate properly and meet the performance specifications listed in this document. If these conditions are not met, the SiP will not perform as expected, but will also not suffer permanent electrical damage.

Table 7: SiP Operating Conditions

Parameter	Min	Typ	Max	Unit	Conditions
VDD_SUP/IO_FLASH voltage	2.375	2.5 or 3.3	3.465	volts DC	All supplies in this row should be at the same voltage Typ column lists common voltages
VDD_DIG/_ANA voltage	1.52	1.6, 2.5, or 3.3	3.465	volts DC	All supplies in this row should be at the same voltage VDD_DIG must be ≤ VDD_SUP Typ column lists common voltages
VCC_PA	3	3.3	5	volts DC	Typ column lists operating at 25dBm
Opertating Temperature	-40	N/A	85	°C	Analysis performed using worst case power consumption and a specific PCB layout (TBD)

2.4.3 Radio Functional Specifications

The main radio functional specifications are reference to ImpinjI Ex10 specifications.

Table 8: SiP Power Consumption

Parameter	Min	Typ	Max	Unit	Conditions
SiP performing inventory, transmitting at +25 dBm Note: SJC does not increase power consumption.		2700		mW	3.3V single supply
SiP idle		130		mW	3.3V single supply
SiP disabled		0.5		mW	3.3 V single supply, ENABLE deasserted
SiP held in reset			50	mW	Using RESET_N pin

Table 9: SiP Radio Overall Specifications

Parameter	Min	Typ	Max	Unit	Conditions
Tag read rate	N/A	*900		Tags / second	Note: This is the maximum read rate the chips are capable of, and firmware support for this read rate will arrive in a future version.
Forward Link Modulation	N/A	N/A	N/A		DSB-ASK PR-ASK
Forward Link TARI	6.25	N/A	25	us	Configurared by RF Mode
PIE Ratio	1.5	N/A	2		Configurared by RF Mode
Reverse Link Frequency (BLE)	40	N/A	640	KHz	Configurared by RF Mode

Table 10: SiP RF Mode

Mode ID*	Mode Optimization	Forward Link Modulation	Tari (µs)	PIE	BLF (kHz)	Reverse Link Modulation	SiP Sensitivity**			Maximum Read Rate***
							MS710	MS510	MS310	
103	Read Rate	DSB-ASK	6.25	1.5	640	FM0	-78	NA	NA	1000+
302	Read Rate	PR-ASK	7.5	2	640	FM0	-78	NA	NA	800+
120	Read Rate	DSB-ASK	6.25	1.5	640	Miller M=2	-81	-75	NA	700+
323	Read Rate	PR-ASK	7.5	2	640	Miller M=2	-81	-75	NA	550+
202	Read Rate	PR-ASK	15	1.5	426	FM0	-79.5	NA	NA	500+
345	Read Rate	PR-ASK	7.5	1.5	640	Miller M=4	-84	-75	NA	400+
344	Read Rate	PR-ASK	7.5	2	640	Miller M=4	-84	-78	NA	400+
223	ETSI	PR-ASK	15	2	320	Miller M=2	-84	-78	-71	300+
222	ETSI	PR-ASK	20	2	320	Miller M=2	-84	-78	-71	250+
241	ETSI DRM	PR-ASK	20	2	320	Miller M=4	-87	-81	-74	200+
244	FCC DRM	PR-ASK	20	2	250	Miller M=4	-88	-82	-75	150+
285	Sensitivity	PR-ASK	20	2	160	Miller M=8	-93	-87	-80	50+

*Reader mode availability shown for Impinj Reader Chip SDK+FW version 1.2

**1% Packet Error Rate, with +10 dBm self-jammer at MS710, MS510, or MS310 RX pin, DC blocking baseband filter (not DRM), typical Gen2 parameters
***Tag read rates shown are for a large tag population in a quiet RF environment, using the MTI MS710 Development Board. MTI MS510 and MS310 reader SiP are typically lower.

Table 11: SiP Receiver Specifications

Parameter	Min	Typ	Max	Unit	Conditions
Input Frequency	860		930	mW	RX port
Input Impendance		50		Ohm	RX port
Return Loss	10				RX port
RX port self-jammer power			11	dBm	Must also be 24 dB or more below internal coupler input power 35dBm at CPL_TI if RX self-jammer is +11dBm
Sensitivity		See Table 10		dBm	
RSSI measurement accuracy		3		dB	After per-board RSSI calibration
Phase measurement accuracy		+/-5		Degrees	Phase measurements have 180 degrees of phase ambiguity in non-FM0 modes

Table 12: SiP Transimter Specifications

Parameter	Min	Typ	Max	Unit	Conditions
Embedeed Ex10					
Maximum TX power output capability at YK_TO port	11			dBm	
TX output power regulatory compliant range	5		11	dBm	Across this chip output power range, regulatory compliance is guaranteed with external amplification up to the maximum power allowed in the region Below this range, reader overall output power must be reduced by 1 dB per 1 dB of chip transmit power to meet regulatory compliance
TX output power analog dynamic range	30			dB	Note: Optimal spectral performance is achieved at maximum chip TX power.
TX port analog power step size		1		dB	Note: Digital power control offers finer control
TX power digital control resolution		12		Signed bits	Linear control, full scale achieves maximum TX output power For more detail, see the MTI MSx10 RFID Reader Calibration Application Note

Parameter	Min	Typ	Max	Unit	Conditions
Internal PA					
Maximum TX power input capability at PA_TI port			10	dBm	
Maximum TX power output capability at PA_TO port	25			dBm	
Internal PA Gain		26		dB	at PA_TO pin, VCC_PA is 3.3V
Internal PA P1dB		29		dBm	at PA_TO pin, VCC_PA is 3.3V
RFFE					
Insertion Loss		1.2		dB	CPL_TI to ANT
Isolation		30		dB	CPL_TI to CPL_RO
Max input power at CPL_TI			3	W	
Harmonic rejection		30		dB	at 2nd & 3rd harmonic band

Table 13: SiP Power Dector

Parameter	Min	Typ	Max	Unit	Conditions
CPL_TI power detector input	2		33	dBm	to internal LO power detector
RX power detector input	-15		18		
RX and CPL_TI power detector accuracy		+/- 0.5		dB	After calibration CPL_TI input power +21~33dBm RX Input power +4 to +17 dBm
		+/- 1.0		dB	After calibration CPL_TI input power +11~+21dBm RX Input power -6 to +4 dBm

Table 14: SiP Transimter Synthesizer

Parameter	Min	Typ	Max	Unit	Conditions
Frequency Range	860		960	MHz	
Frequency Grid		100 125 250		KHz KHz KHz KHz	Europe (ETSI 302 208) EU1, EU2, Japan China, Korea USA (FCC)
Reference input frequency		24		MHz	TCXO Specification
Reference frequency tolerance			10	ppm	TCXO Specification
Reference input level	0.5		1.5	V	AC Coupled clipped sine wave

2.4.4 Auxiliary Analog Specifications

Table 15: SiP Auxiliary ADC Specifications

Parameter	Typ	Unit	Conditions
Input Minimum	0	Volts	
Input Maximum	1	Volts	
Resolution	10	Bits	Full scale
DNL	2	LSB	
INL	4	LSB	
Input Impedance	10	kOhms	Measured relative to ground
Sample Rate	100	Ksps	Limited by host communication rate

Table 16: SiP Auxiliary DAC Specifications

Parameter	Typ	Unit	Conditions
Resolution	10	Bits	Full scale
Current Mode Output Minimum	0	uA	
Current Mode Output Maximum	100	uA	
Current Mode DNL	2	LSB	
Current Mode INL	2	LSB	

2.4.5 IO Functional Specifications

Table 17: SiP Digital IO Specifications

Parameter	Min	Typ	Max	Unit	Conditions
Input high voltage	2		VDD_IO_FLASH	V	Input high voltage levels
Input low voltage	-0.3		0.8	V	Input low voltage levels
Output high voltage	VDD_IO_FLASH - 0.1			V	Output high voltage
Output low voltage			0.4	V	Output low voltage
Output sink and source current	4			mA	
IO pull up resistance	34	51	81	kOhms	

2.4.6 Host SPI Interface Functional Specifications

Table 18: SiP Digital IO Specifications

Parameter	Max	Unit
SPI Host Clock Frequency – Active Mode	4	MHz
SPI Host Clock Frequency – Bootloader Mode	1	MHz

3 FUNCTIONAL DESCRIPTION

The MTI MSx10 is an Impinj Ex10 based RFID reader SiP. The below description are accosiated with Impinj Ex10 reader chip.

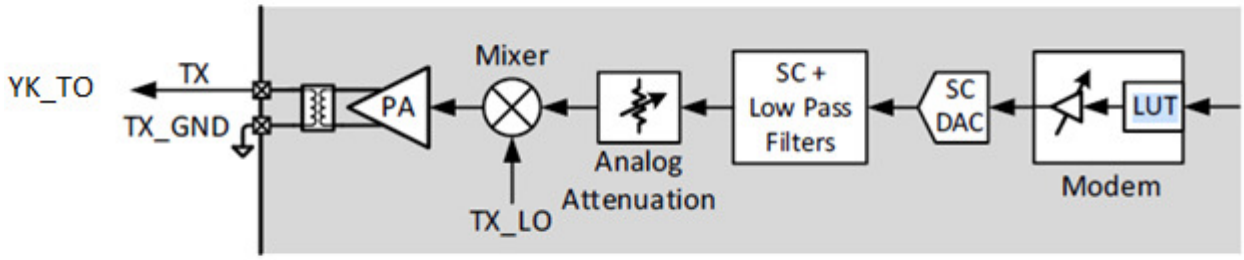
3.1 Analog Transmitter Path

The embedded Impinj E710, E510, and E310 contain the entire digital and analog TX signal chain required to transmit up to the maximum transmit power of the chips, as specified in Table 11: Chip Transmitter Specifications. This signal chain is shown in Figure 10. An external power amplifier may be used in applications where additional transmit power is required.

The transmitted waveform is generated inside the modem, where a lookup table contains a sequence of digital values. Those digital values go through a digital multiplication with a signed 12-bit gain value (also known as “fine gain”). After the digital multiplication, the values enter a switched capacitor (SC) digital to analog converter (DAC), and exit as an analog waveform. The analog waveform goes through switched cap and low pass filters before an analog attenuation stage. The analog attenuation (also known as “gross gain”) has 30 ~1 dB attenuation steps. After attenuation, the analog waveform is mixed with the transmit local oscillator (TX_LO), and then amplified by the internal PA, and finally output through a balun as a single ended signal on the TX pin.

The embedded Impinj E710, E510, and E310 produce optimal spectral performance when the internal power amplifier is operated at the maximum allowable power (~11 dBm) at YK_TO. The internal analog and digital gain can be reconfigured at runtime to cover a wide power range. Given the optimal spectral performance at high output power, the reader chip and surrounding circuitry, including external PA bias, should be configured to target maximum reader output power at the maximum chip output power. Then the overall output power can be reduced to lower values by reducing the internal chip PA gain.

Figure 9 – Transmitter Front End Analog Circuitry

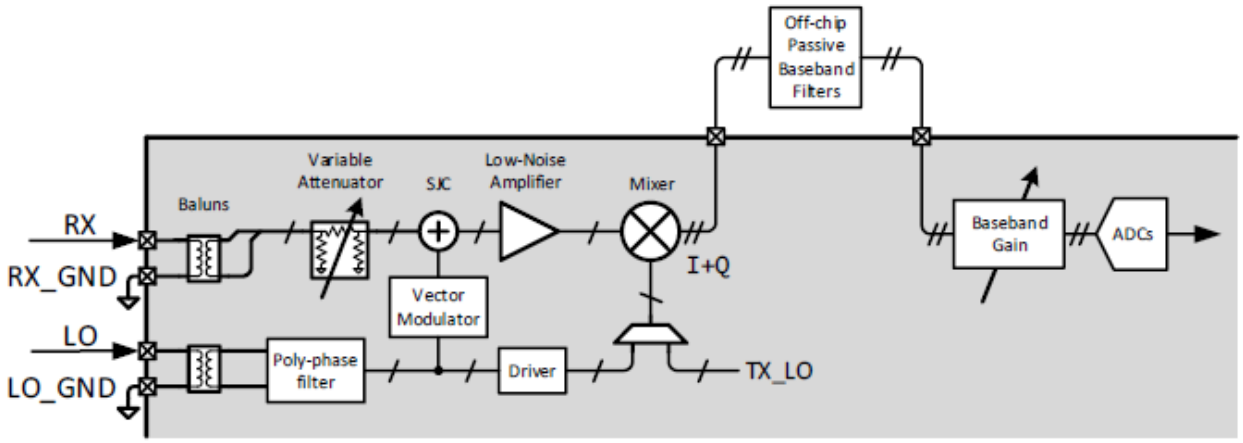


3.2 Analog Receiver Data Path

3.2.1 Receiver Front End Circuitry

The Receive (RX) and Local Oscillator (LO) RF inputs to the embedded Impinj E710, E510, and E310 chips are single ended.

Figure 10 – Receiver Front End Analog Circuitry



3.2.2 Local Oscillator Input

The Local Oscillator (LO) input is from internal directional coupler.

3.2.3 Self-Jammer Cancellation Block

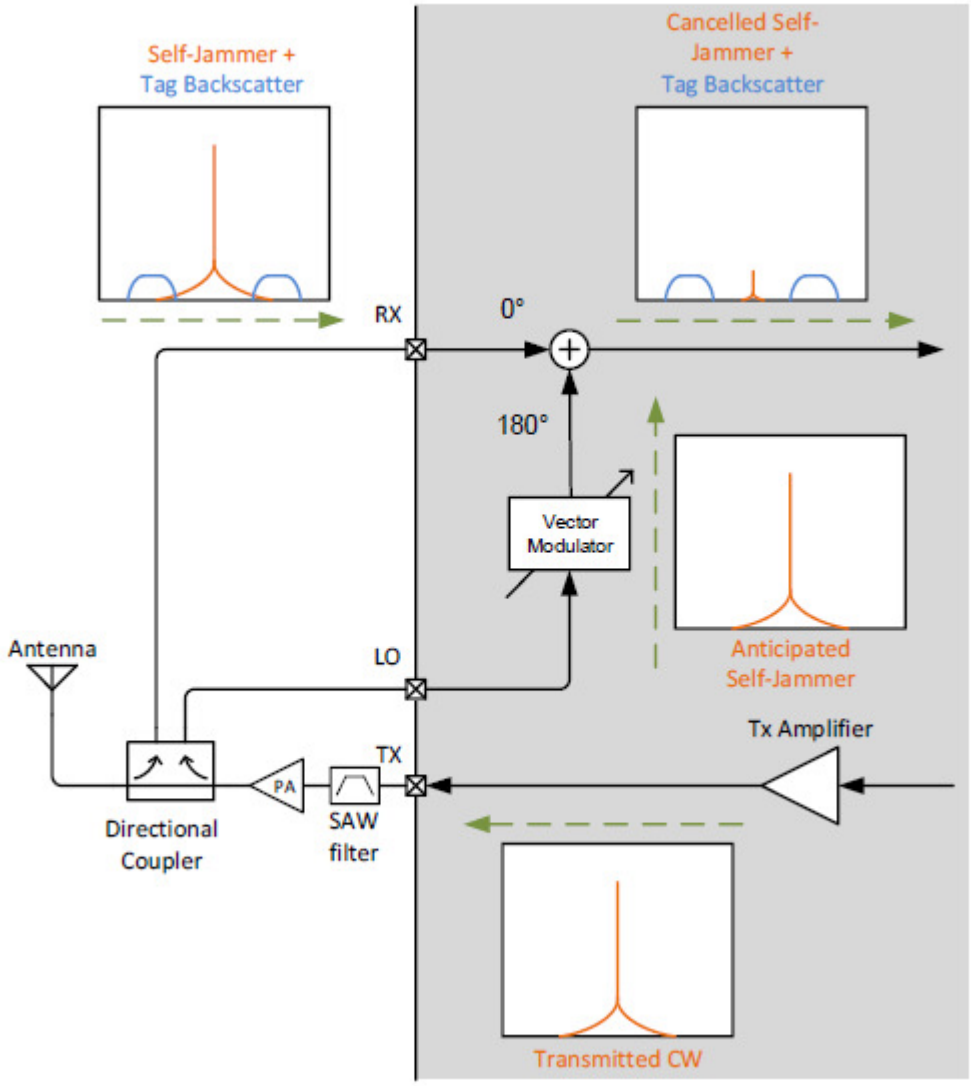
The embedded Impinj E710, E510, and E310 chips contain self-jammer cancellation (SJC) circuitry to improve receiver sensitivity. This circuit effectively reduces the negative impact of antenna reflection of the transmitted carrier wave (CW) on the receiver's sensitivity. RAIN systems using monostatic antenna configurations suffer from self-jammer problems because the transmitter must transmit CW continuously while the tags are backscattering their reverse link signal. That transmitted CW will reflect off of the antenna, resulting in a self-jammer signal incident at the receive port of the reader chip. That self-jammer signal will be much larger in amplitude than the reverse link signal from the tags.

The next-generation SJC block in the embedded Impinj E710, E510, and E310 iterate upon the SJC block developed in the Impinj Indy R2000 chip, reducing current consumption by implementing passive self-jammer cancellation, and improving sensitivity by increasing the resolution of the vector modulator circuit.

The embedded Impinj E710, E510, and E310 perform self-jammer cancellation by converting the Local Oscillator (LO) signal into an anticipated reflected CW and subtracting it from the Receive (RX) signal, using the Vector Modulator and other components shown in Figure 10. An example of the complete signal chain and resultant receive signal spectrum is shown in Figure 11.

Proper operation of the SJC requires that the LO signal have the proper amplitude as it enters the embedded Impinj E710, E510, and E310.

Figure 11 – Self Jammer Cancellation Spectrum



3.2.4 Receive Baseband Interface

After the self-jammer signal is removed from the receive signal, the resulting RF signal is demodulated using the LO, resulting in a quadrature baseband signal. This signal is then filtered to remove out of band frequency content. The unfiltered signal is output from the chip on the differential quadrature MIX_... pins, and after external passive baseband filtration, it re-enters the chip through the differential quadrature AMP_... pins. The filtered baseband signal is then further amplified and filtered inside the chip, and finally digitized in on-chip ADCs to be processed by the modem. This arrangement is shown in Figure 12.

The component topology and values for the off-chip baseband filters vary by application. For recommendations, see the MTI MSx10 Development Board Application Note. In some configurations, baseband signal filtering is not required, but in all cases the design should have at minimum DC blocking capacitors to interface between the receive mixer and the amplifiers before the ADC.

The SiPs have a single set of differential quadrature input and output pins, so if multiple passive filter networks are desired, external RF switching must be added to the circuit, as shown in the MTI MSx10 development board.

The individual mixer output and amplifier input pins each have a configurable series resistor inside the part, with a resistance of either 250 or 1000 Ω, as configured by the firmware. This is shown in Figure 13.

Figure 12 – Receive Baseband Interface

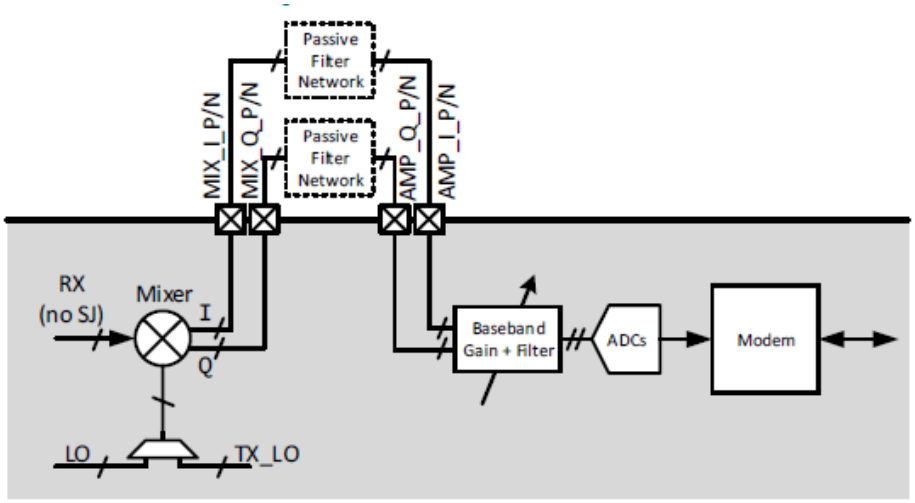
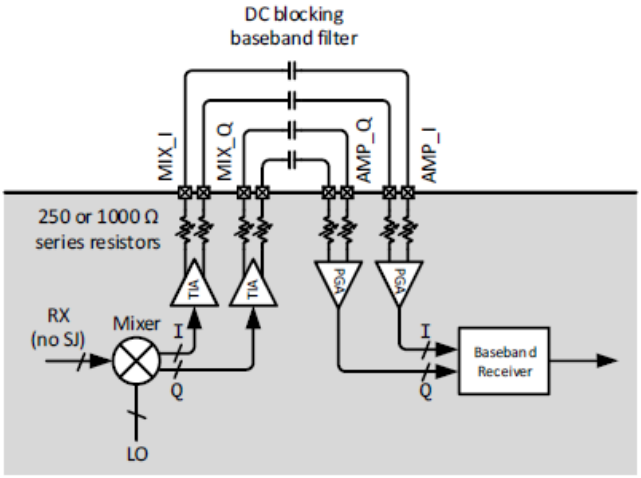


Figure 13 – Receiver Baseband Filter Pin Interface Detail



3.3 Antenna Configuration Scenarios

The MTI Mx10 SiP can be configured for monostatic (single antenna used for both transmit and receive) or bistatic (separate antennas used for transmit and receive) operation. Monostatic configurations are generally more popular, because of the lower cost and size of a single antenna system, but bistatic configurations have the advantage of increased receive sensitivity due to the lack of a reflected self-jammer signal on the receive antenna.

The MTI Mx10 SiP can also be configured for operation with multiple monostatic antennas, for example in a system with multiple physical zones, each with their own antennas. This can be accomplished using an external RF switch, also known as a multiplexer (mux), at the transmitted port of the directional coupler. The RF switch can be controlled by specific GPIOs.

Figure 14 – Monostatic Antenna Configuration

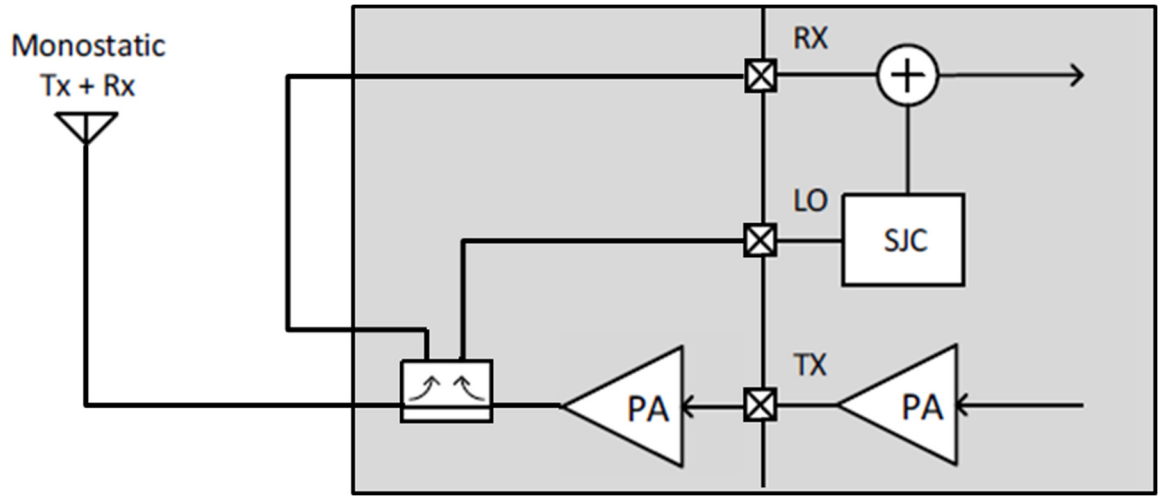


Figure 15 – Bistatic Antenna Configuration

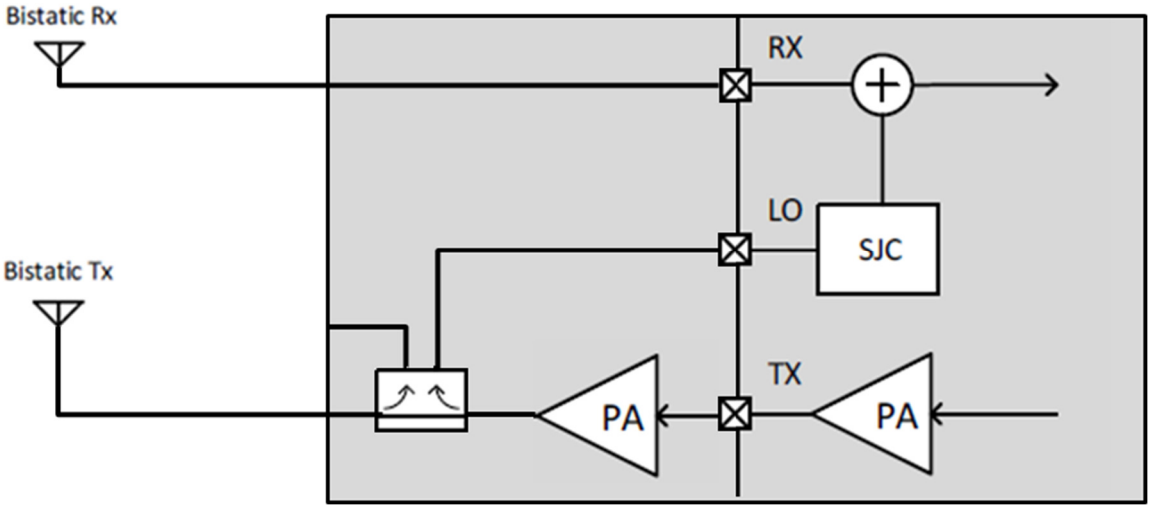
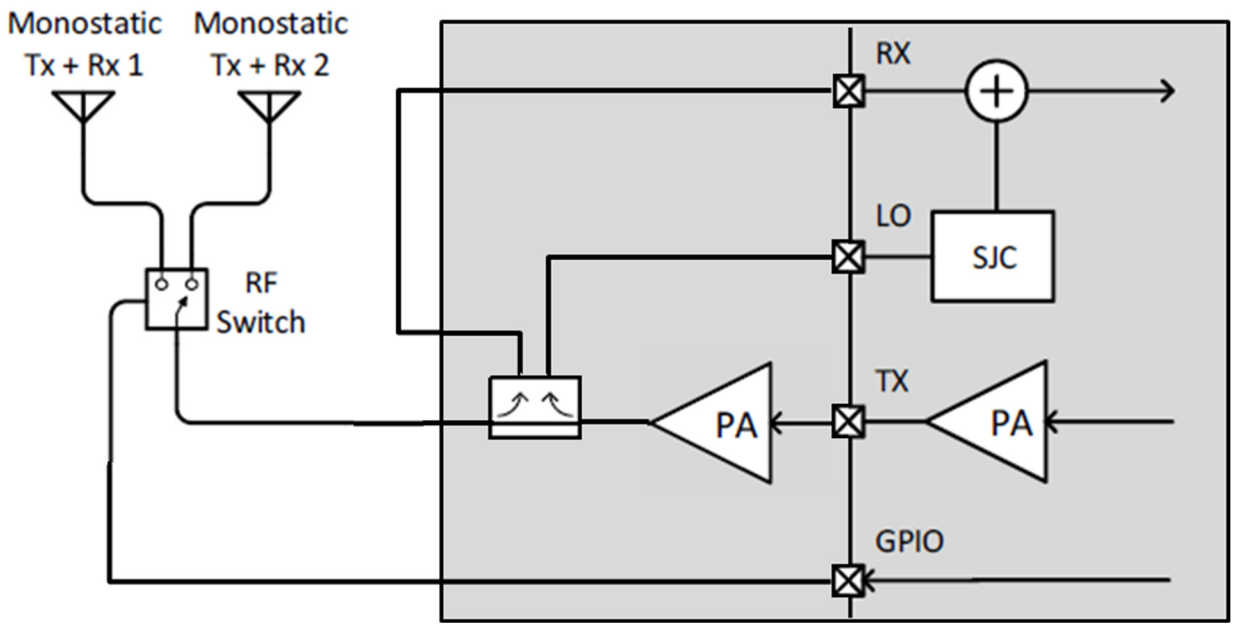


Figure 16 – Multiple Monostatic Antennas with RF Switch



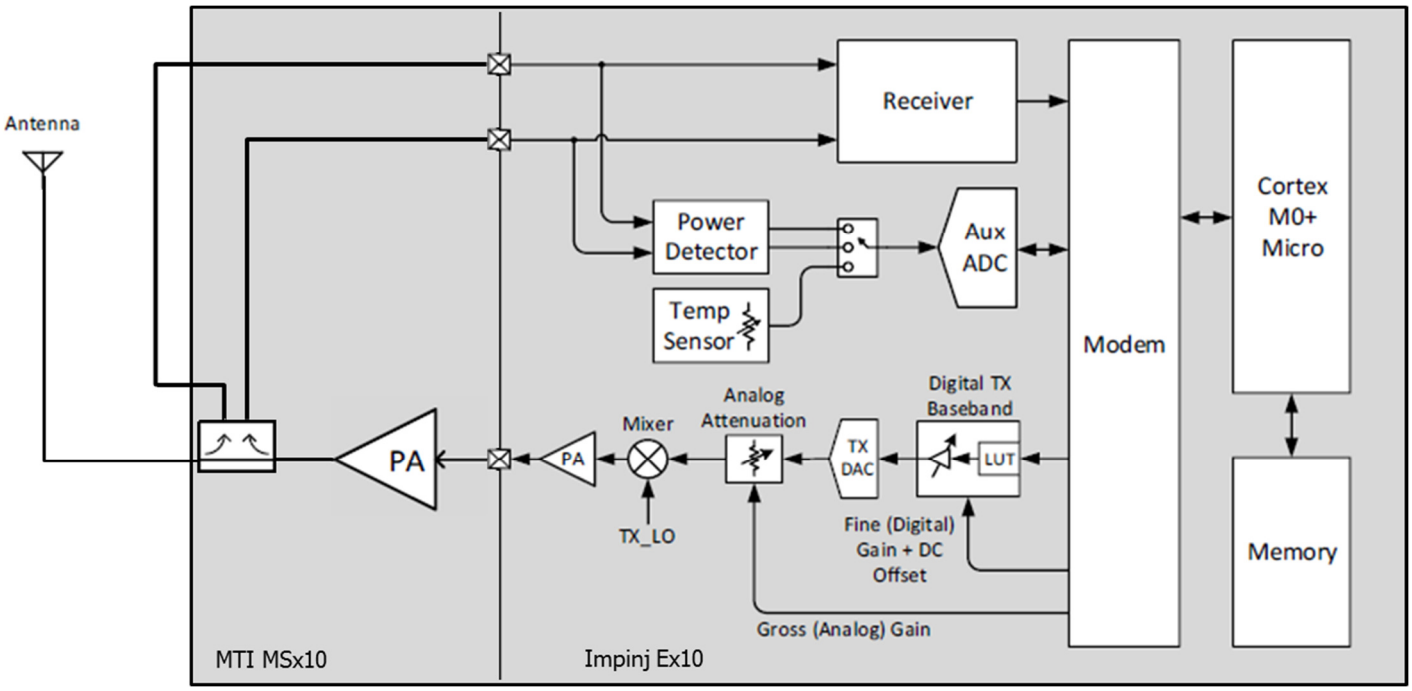
3.4 RF TX, LO, and RX Path Configuration

The MTI Mx10 SiP has implemented with the RF front end circuitry inside, it is easier to connect the transmit (TX), local oscillator (LO), and receive (RX) pins to the antenna(s) via internal RF Front End circuitry to successfully implement a RAIN RFID reader. This circuitry potentially includes attenuators, one or more SAW filters, DC blocking series capacitors, one or more power amplifiers, optional RF switches, and passive filters. All these components serve different purposes that are explained in detail in the MTI MSx10 Development Board Application Note.

3.5 RF Power Detection

The MTI MSx10 SiPs contain power detectors connected to the RX and LO pins, allowing measurement of forward (transmit) power on the LO pin and reverse (self-jammer) power on the RX pin. These power detectors convert the RF power level at the RX and LO pins into an analog voltage, which is measured by the Auxiliary ADC inside the reader chips. The LO power measurement is used to calculate the forward power, for closed loop transmit power control via the fine and gross gains in the transmitter. This arrangement is shown in Figure 17. Both sensors must be calibrated in circuit because circuit design and component values will alter the transfer function between the desired quantities and the power at the reader chip pins. For more detail on calibration and closed loop power control, see the MTI MSx10 RFID Reader Calibration Application Note

Figure 17 – Embedded Impinj Ex10 Circuit Block Diagram With Sensors



3.6 Frequency Generation

3.6.1 Temperature Compensated Crystal Oscillator

The MTI MSx10 SiPs require a high accuracy clock reference signal from an external temperature compensated crystal oscillator (TCXO) to be used as a reference for the VCO and PLL internal to the SiP. The TCXO clock output signal is fed into the reader SiP via the high impedance TXCO_IN pin. The TXCO_IN pin requires AC coupling to remove the DC bias voltage of the TCXO output. The Impinj E710 development board uses a 1 nF capacitor, but other TCXOs may require a different component value. Some TCXO components require a specific load to operate, and this may require external passive components to implement.

TCXO selections should meet the requirements listed in the electrical specifications, specifically Table 14, including the frequency, PPM error, and output waveform's shape and peak to peak voltage. If the peak-to-peak voltage exceeds the specifications of the reader chip, it can be reduced using a voltage divider circuit before the AC coupling capacitor. If necessary, Impinj recommends using a resistor voltage divider with a series resistance of 1 kΩ, and an appropriately scaled shunt resistance for the waveform amplitude. If the waveform shape is not a clipped sine wave, for example a CMOS or HCMOS square wave, it may need to be low-pass filtered using an RC circuit to reduce higher order frequency content, as these can couple into the transmitter and receiver and degrade performance. The TCXO power supply can likewise contain high frequency noise and may require some electrical isolation from the reader circuit.

An example TCXO circuit is shown in Figure 18.

Other TCXO specifications that may matter in the reader system include startup time, power consumption, frequency stability over time, voltage, temperature, and load, etc. These specifications must be considered in reader design, as they may have design implications.

Some TCXO devices are "pullable" meaning a voltage can be applied to one of their pins to shift the operating frequency. This may be used as a mechanism of frequency calibration. If this behavior is not

desired, the pin should be driven to the appropriate DC value to disable frequency pulling.

Recommand TCXOs with success:

- TaiSaw TX0283D
- TXC 7Q-24.000MBN-T
- Taitien TXEABLSANF-24.000000
- Abracon ASTX-H11-24.000MHZ-T

Note: Requires an output voltage divider to achieve <1.5 VP-P input level

3.6.2 Voltage Controlled Oscillator

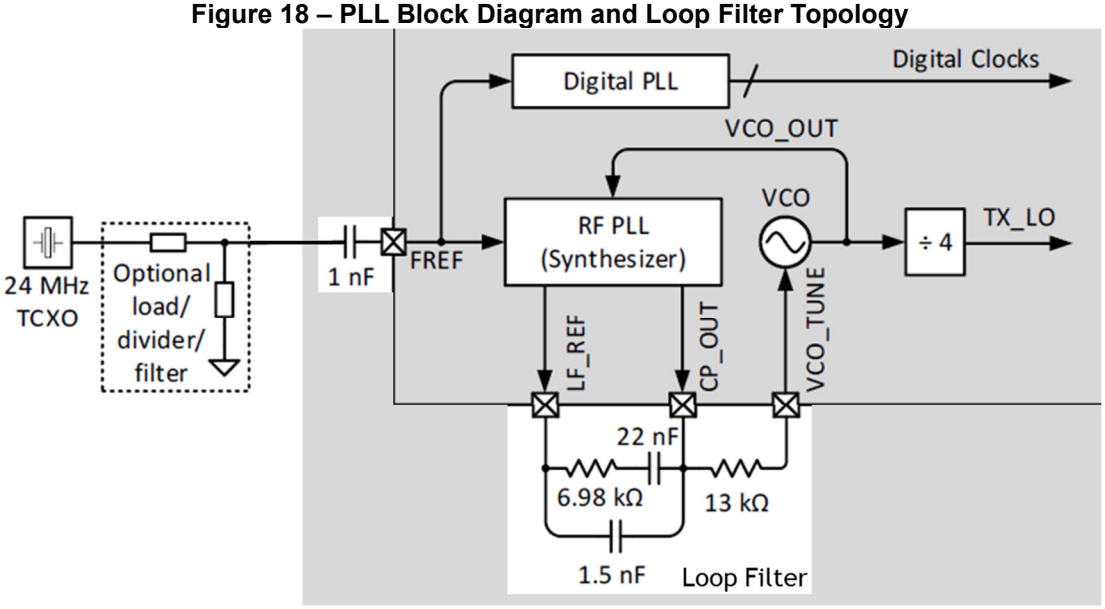
The MTI MSx10 SiPs contain a voltage-controlled oscillator (VCO) that generates a ~3.6 GHz reference signal that is subsequently divided by 4 to generate the carrier wave (CW) signal used for RF transmission, also known as the Transmit LO (Local Oscillator) signal. This reference signal is tunable, allowing the reader chips to operate in different channels in multiple regulatory regions. The VCO is tuned using closed loop feedback from the phase locked loop (PLL), using the TXCO as a reference clock.

The VCO and PLL circuits are configured by the reader chips' embedded firmware image. The SPI host can interact with this configuration via Operations and Register values. This is demonstrated in the SDK's examples, as described in the Impinj Ex10 Reader Chip SDK Specification.

3.6.3 PLL Loop Filter

The PLL Loop Filter circuitry has implemented into MSx10 SiP

Figure 18 – PLL Block Diagram and Loop Filter Topology



3.7 Power Modes

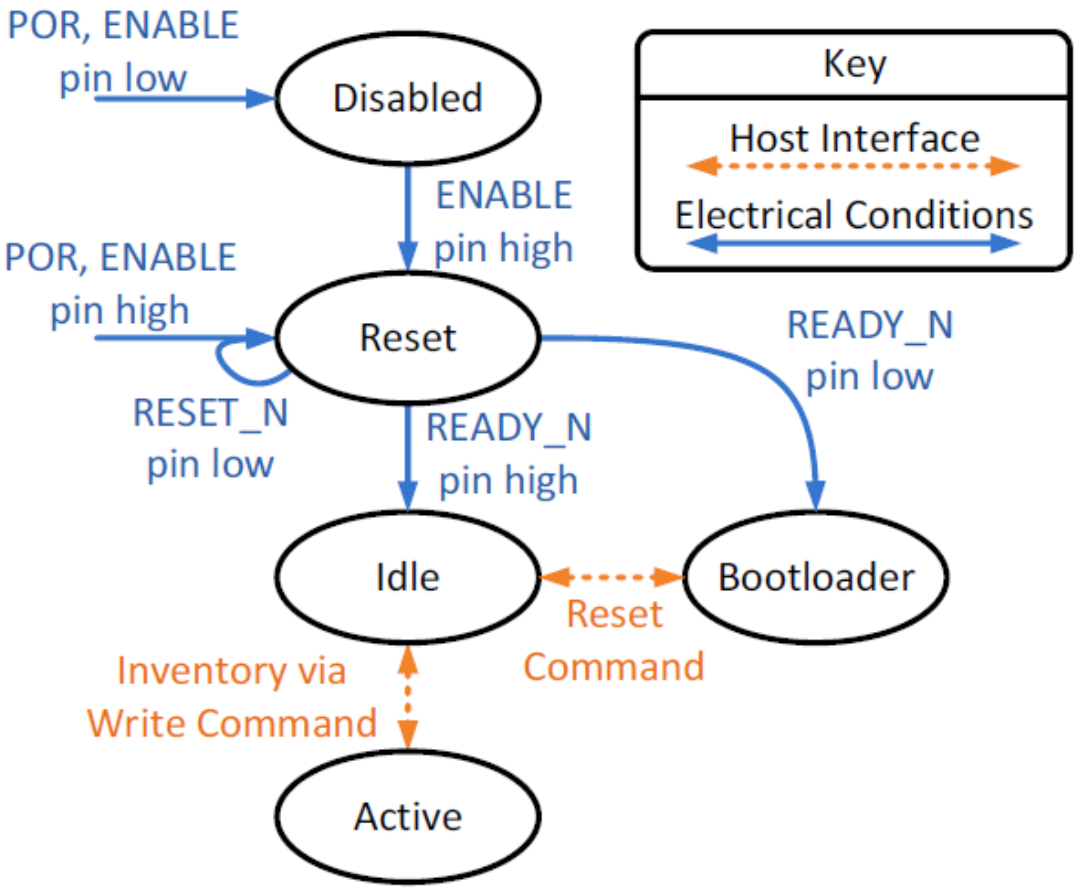
The MTI MSx10 SiPs have multiple operating modes, allowing power consumption and performance optimizations for all applications. The power modes and transitions between them are shown in Figure 19. Power consumption characteristics of the modes are shown in Table 7.

When power is applied to all of the power supply pins on the chip, it will enter either Disabled or Reset power mode, depending on the state of the ENABLE pin. If the ENABLE pin is low, it will enter the Disabled mode, but if the ENABLE pin is high, it will enter the Reset mode. From the Reset mode, if the RESET_N pin is high, the chip will transition into either the Idle or Bootloader mode, depending on the state of the READY_N pin.

The READY_N pin can be driven low to force the chip into the Bootloader mode or left high to allow the chip to boot into Idle mode. From Idle mode, the chip can be sent into the Active mode(where RFID operations are performed) or Bootloader mode, depending on commands sent via the host interface. The RESET_N pin can be used at any time to force the chip into the Reset mode or keep it there indefinitely. Setting the ENABLE pin low will force the chip into the Disabled power mode, which consumes less current than any of the other power modes. Refer to section 2.3 - Power Supply for details on power mode transitions.

The MTI MSx10 SiPs do not have an independent internal clock source, and if no 24 MHz clock signal is provided at the FREF input, the parts will not start up.

Figure 19 – MTI Reader SiP Power Modes



4 DEVICE CONTROL AND PROGRAMMING

The MTI MSX10 has an embedded Cortex-M0 microcontroller that runs RAIN application specific firmware. That firmware implements the behavior necessary to operate the RAIN radio and exposes an interface for communication with a host device. The host device communicates with the SiP over an SPI channel, implementing a specific communication scheme that is explained further below. MTI provides explicit documentation of the “wireline” details of the protocol, enabling users to implement their own code to communicate with the SiP. MTI also provides an example implementation of a host library designed to communicate with the SiP.

The MTI MSX10’s embedded microcontrollers can only run the MTI provided firmware images and will not execute any other application code. The SiP exposes a firmware update interface (bootloader), so that newer versions of the firmware can be installed on the SiP, adding new features, fixing bugs, etc. In addition to the RAIN behavior, the firmware also implements test and calibration functionality, and allows the non-volatile storage of calibration configuration, as well as stored configurations for RAIN behavior.

The MTI MSX10 is populated with a firmware image during MTI’s manufacturing and test process. MTI will populate the MSX10 with the latest major revision of firmware. The major revision is updated when large changes are made to the host interface, new devices are added to the MTI MSx10 family, or major bugs are fixed. These major revision updates will be communicated to customers via PCN. MSX10 devices should include the capability to update the firmware image on the MSX10 in the field, so that bugs can be removed and new features can be added. Firmware update can also be implemented in MSX10 based reader manufacturing flow, if a specific firmware image version is desired. For more information on performing firmware updates, see the MTI MSx10 Reader SiP SDK Specification.

Further detail on the behavior of the embedded microcontroller is contained within the MTI MSX10 firmware datasheet (in development). This document contains information on the structure of the data that is sent across the SPI communication interface, as well as the commands and responses that can be exchanged.

It also contains a map of the registers that are used to read and write device configuration. It will document the functional behavior of the SiP, including all the different operating modes the device supports.

4.1 Reader Communication Protocol

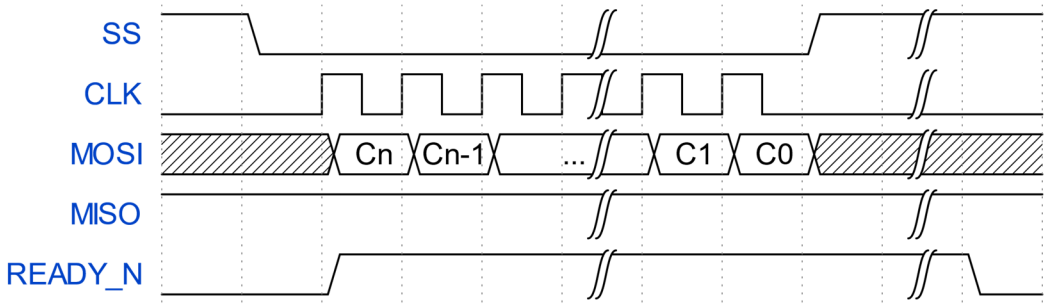
MTI MSX10 reader communication with an SPI master host uses bytes that are sent across the SPI interface to build messages. These messages can describe commands from the host to the SiP, and optionally responses from the SiP to the host. Commands begin with a single “ID” byte, and responses begin with a single “response code” byte, and both are optionally followed by a payload made up of one or more fields of data, each broken up into a number of individual bytes. Not all commands have responses, but they will often change the state of the device registers. More detail on the reader communication protocol is contained in the MTI MSx10 SDK Specification.

4.2 SPI Digital Communication Interface

The MSX10 SiP communicates via SPI (Serial Peripheral Interface). The SiP acts as an SPI slave. The SiP has additional digital IOs that help co-ordinate SPI communication with the host, including the READY_N and IRQ_N pins.

The MSX10 SPI uses 8-bit words, communicated most significant bit first. If multiple bytes are sent, they are sent with the most significant byte first. Both of these are “big endian”. The SPI CPOL = 0, which means the clock signal SCLK idles low. The SPI CPHA = 1, which means the data pins MOSI and MISO states should change on the rising edge of the clock, and be sampled on the falling edge of the clock.

Figure 20 – SPI Master Transaction with No Response



For more details on MSX10 SPI behavior and the host communication protocol, see the MTI MSx10 Reader SiP SDK Specification.

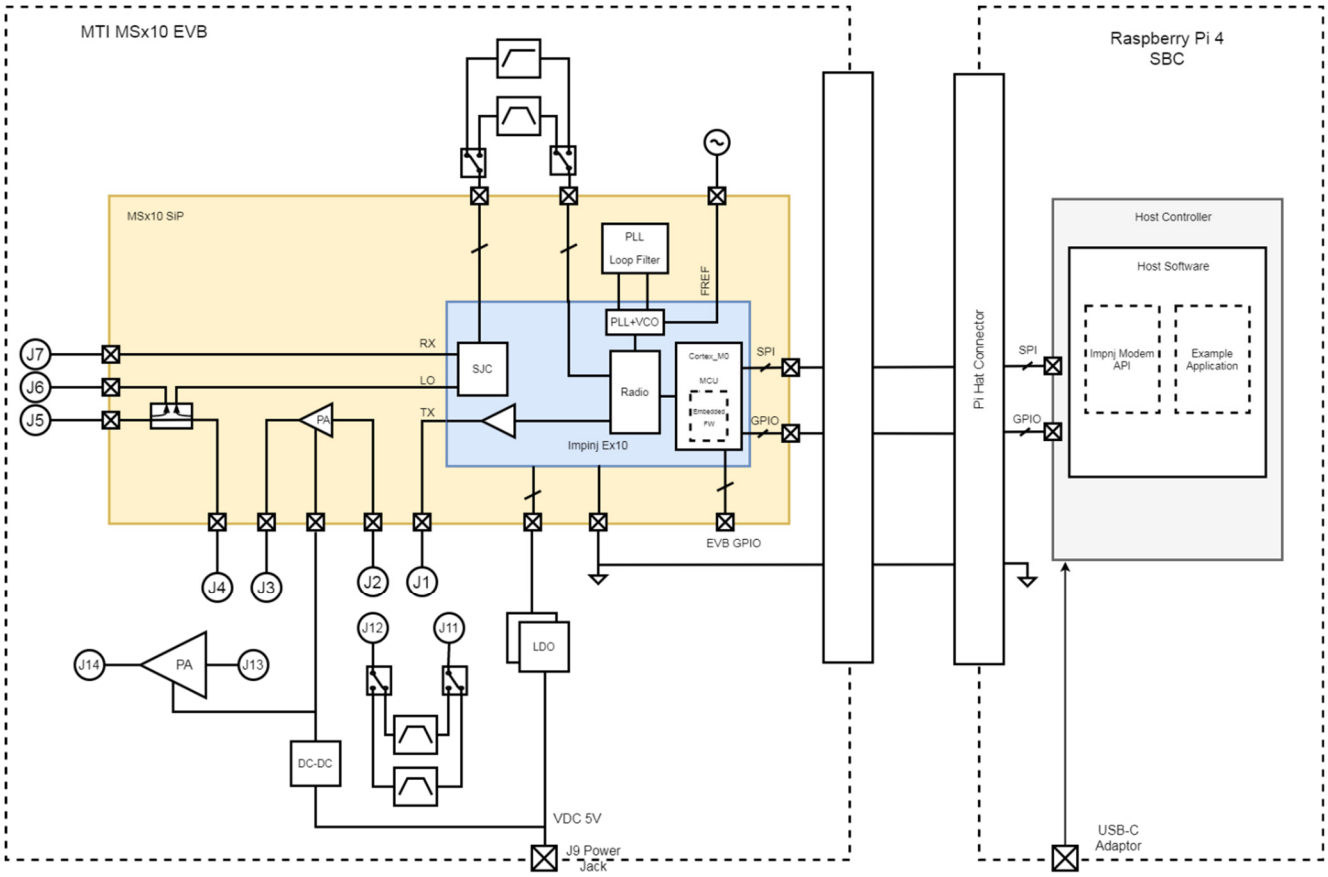
4.3 Digital Input/Output Pins

The MTI Ex10 SiP have Digital Input/Output pins (DIGITAL_IOs) that can be used as digital inputs or outputs in certain configurations, for example for switching between antennas, SAW filters, or baseband receive filters, or reading external voltages. For more detail on controlling the Digital IOs

5 EMBEDDED READER REFERENCE DEVELOPMENT BOARD

For more application specific details on hardware configuration of the MSx10, see the reference design documentation, MTI MSx10 Development Board Application Note

Figure 21 – MTI MSx10 Development Board System Detailed Block Diagram

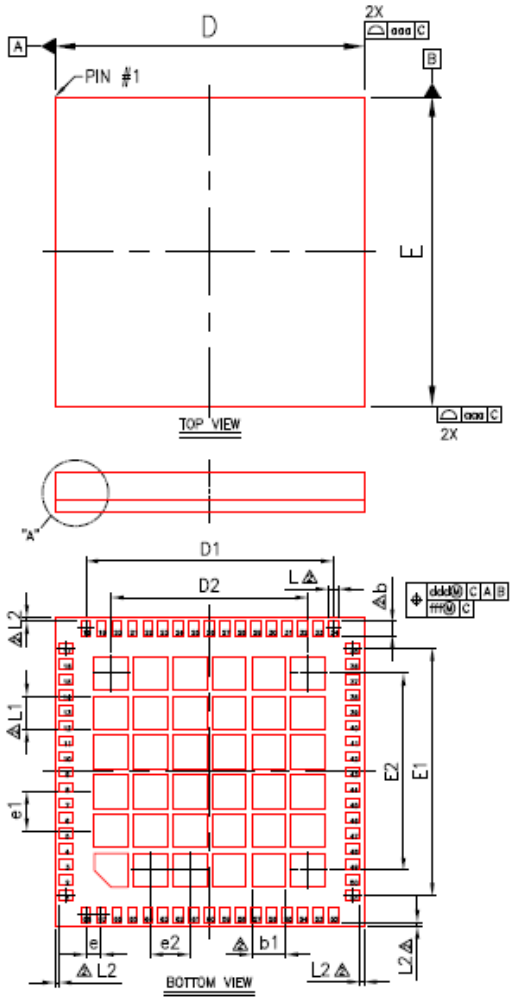


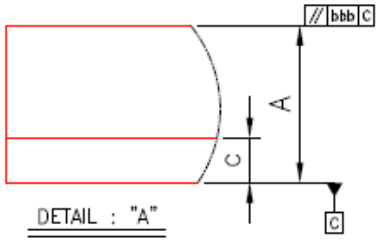
6 PACKAGE AND LAYOUT INFORMATION

6.1 Package Dimensions

The MSx10 SiP is packaged in a 11 x 11 mm, 1.4 mm thick, 68 pin leadless sawn LGA package with a center e-pad that is connected to ground. The package and pin dimensions are shown in Figure 22.

Figure 22 – MSx10 SiP Package and Pin Dimensions





Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.33	1.40	1.47	0.052	0.055	0.058
c	0.36	0.40	0.44	0.014	0.016	0.017
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	---	8.80	---	---	0.347	---
E1	---	8.80	---	---	0.347	---
D2	---	7.00	---	---	0.276	---
E2	---	7.00	---	---	0.276	---
e	---	0.55	---	---	0.022	---
e1	---	1.40	---	---	0.055	---
e2	---	1.40	---	---	0.055	---
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	1.15	1.20	1.25	0.045	0.047	0.049
L	0.30	0.35	0.40	0.012	0.014	0.016
L1	1.15	1.20	1.25	0.045	0.047	0.049
L2	---	0.15	---	---	0.006	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. DIMENSION b,b1,L,L1&L2 IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd.

6.2 PCB Layout Recommendations

Receive sensitivity varies with a number of design parameters, including components used in the baseband filter, power supply topology, selected RF mode, etc. The RX sensitivity of the MSx10 reference design has been captured in the MTI MSx10 Development Board Application Note.

6.2.1 Recommended PCB Footprint

The details please see Development Board design file in SDK

6.2.2 Recommended Reflow Profile

MTI recommends a JEDEC standard J-STD-002D profile with a peak temperature of between 245° C and 250° C

Table 19: Recommended Reflow Profile Parameters

Parameter	Min	Typ	Max	Unit
Temperature Ramp Up Rate			3	° C / second
Preheat Temperature	150		200	° C
Preheat Time	60		180	seconds
Liquidus Temperature		217		° C
Time above Liquidus Temperature	60		150	seconds
Peak Temperature	245		250	° C
Time within 5° C of Peak Temperature	20		40	seconds
Temperature Ramp Down Rate			6	° C / second
Time Between Room Temp and Peak Temperature			480	seconds

7 REFERENCE DOCUMENTS

Table 20: Reference Documents

Document	Description
MTI MSx10 Development Kit User's Guide	Documents how to use the completedevelopment kit, SDK, and host examples, including Quick Start Guide.
MTI MSx10 Development Board Application Note	Documents the MTI MSx10 development board hardware, circuit topologies, design performance, and potential modifications.
MTI MSx10 RFID Reader SiP Datasheet **(this document)**	Documents the MTI MSx10 SiP, including electrical and mechanical specifications.
MTI MSx10 RFID Reader Calibration Application Note	Documents an example procedure and background to calibrate an MTI MSx10 SiP based RAIN RFID reader.
MTI MSx10 MCU Host Porting Application Note	Demonstrates a RAIN RFID inventory example running on a NUCLEO-L433RC-P microcontroller development board host, using the C library included with the MTI reader SiP SDK.

8 DOCUMENT CHANGE LOG

Table 21: Document Change Log

Version	Date	Description
0.6	2020-12-17	First release of preliminary version.
0.8	2021-07-21	1. Rename product name to “MSx10”, 2. Update Section 2.1 Pin Listing and Signal Definitions 3. Update Section 2.4 Electrical Specifications 4. Modify Section 4.1 Package Dimensions
1.0	2021-10-13	1. Update Section 2.4 Electrical specifications 2. Update Figure 6 – MTI MSx10 Startup Power Supply and IO Sequencing 3. Add Section 2.3.2 Power Down Sequence 4. Add Section 2.3.3 Disable-Enable Sequence 5. Update some specs in Section 2.4 Electrical specifications 6. Add Section 3 Function Description 7. Update SiP thickness tolerance in Figure 16
1.1	2022-01-20	1. Update Table 3: MTI MSx10 Signal Listing 2. Add Section 2.4.4 : Auxilliary Analog Specifications 3. Add function descriptions and figures on various topics in section 3 4. Add two documents in REFERENCE DOCUMENTS section ◦ MTI MSx10 RFID Reader Calibration Application Note ◦ MTI MSx10 MCU Host Porting Application Note
1.1a	2022-03-23	1. Add an update code to version control information
1.2a	2022-08-19	1. Added section 2.2.1 - Digital IO Default Drive Modes 2. Update Table 10 : SiP RF mode 3. Add Table 22: SiP Digital IO Specifications 4. Add section 6.2.2 Recommended Reflow Profile

9 NOTICES

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